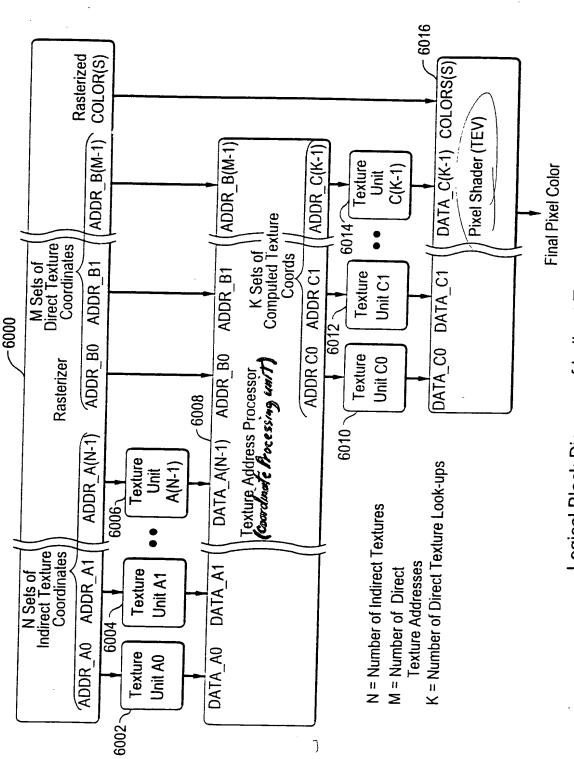
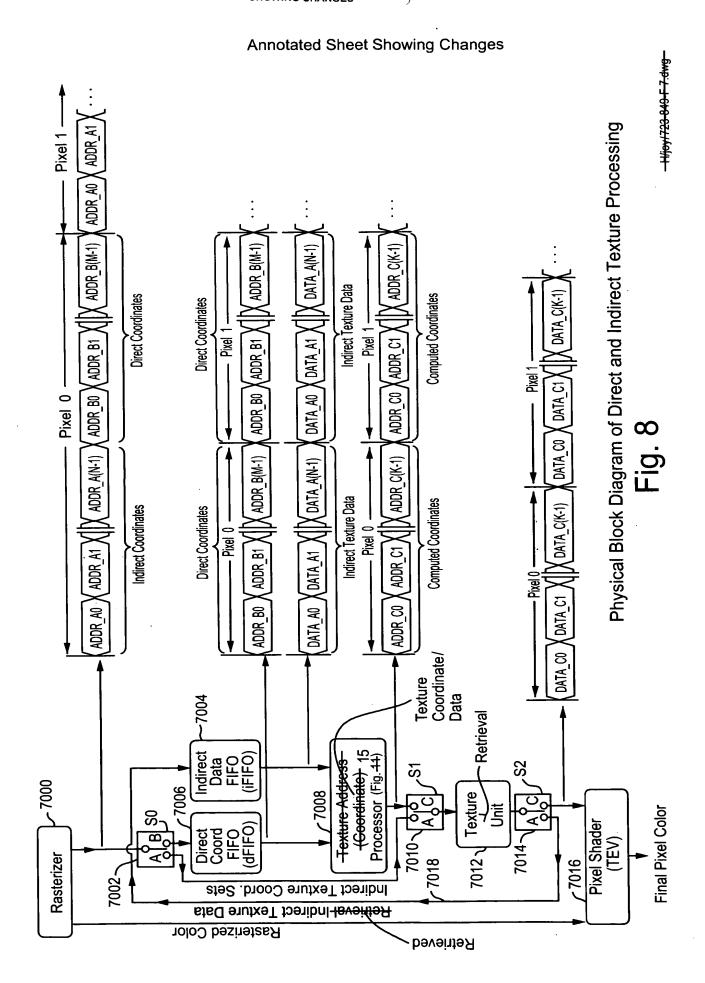
Appl. No. 09/722,382 Atty. Dkt.: 723-961 ANNOTATED SHEET SHOWING CHANGES



Logical Block Diagram of Indirect Texture Processing



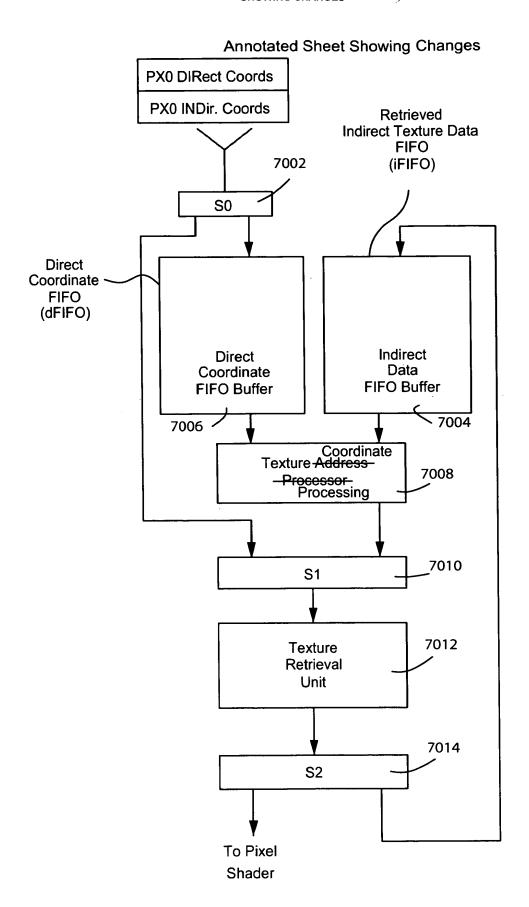


Fig. 10A

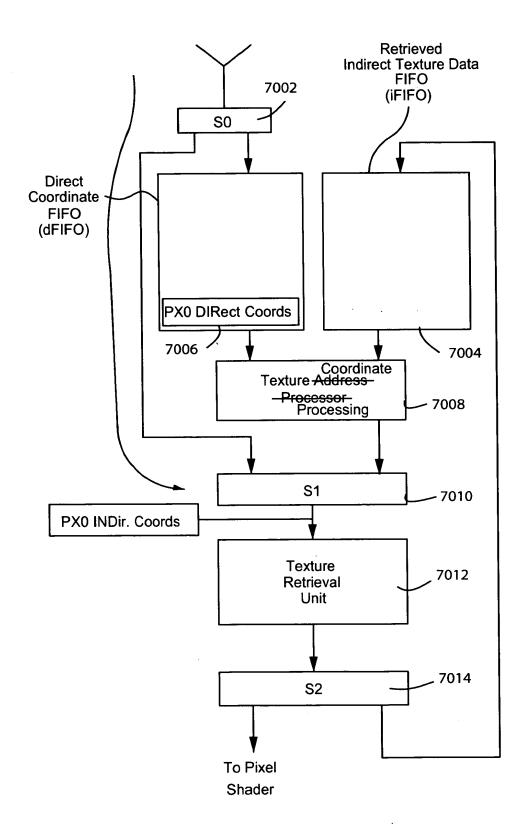


Fig. 10B

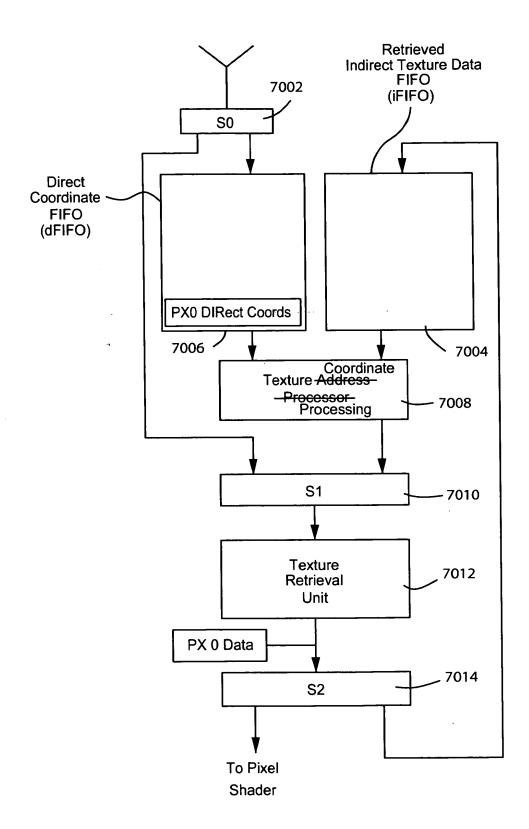


Fig. 10C

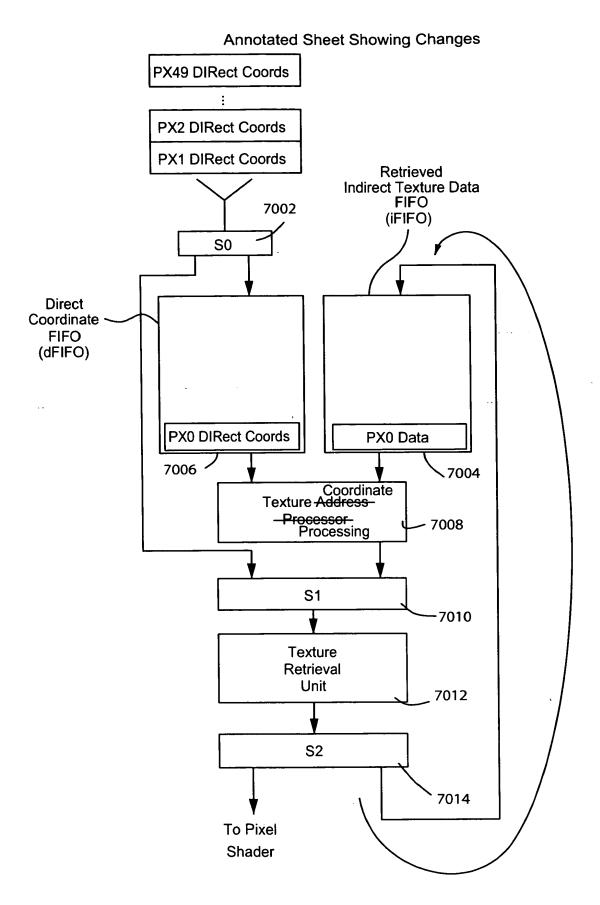


Fig. 10D

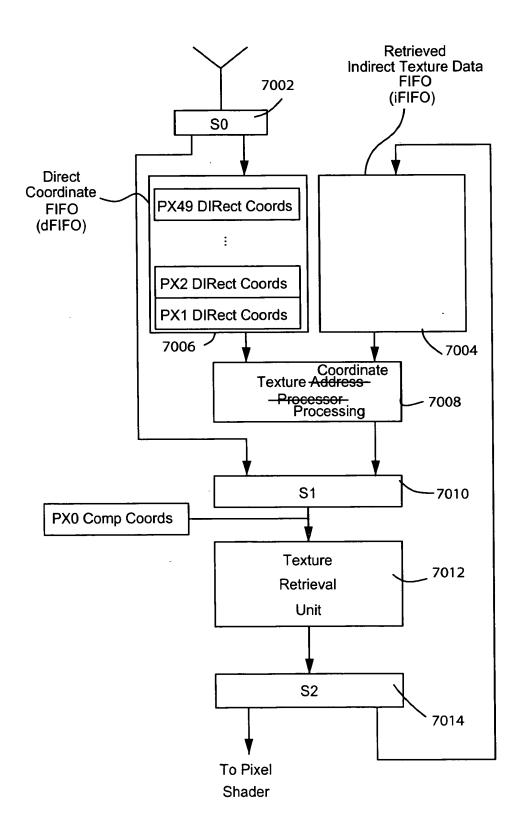


Fig. 10E

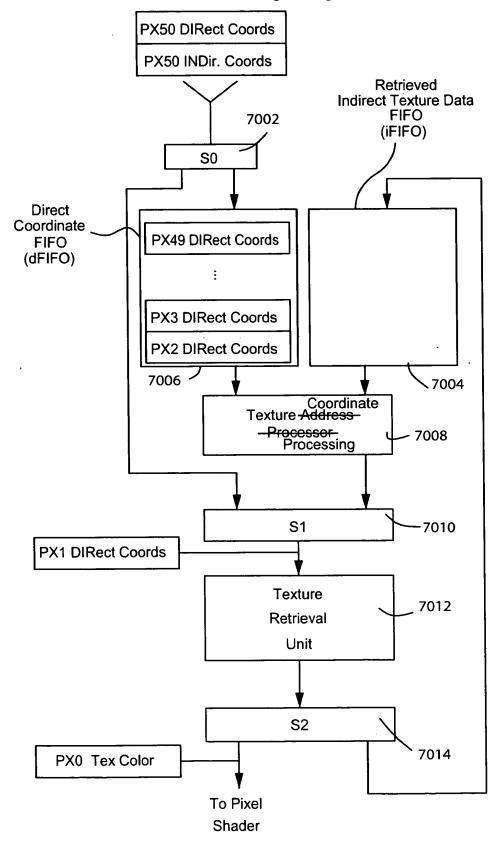


Fig. 10F

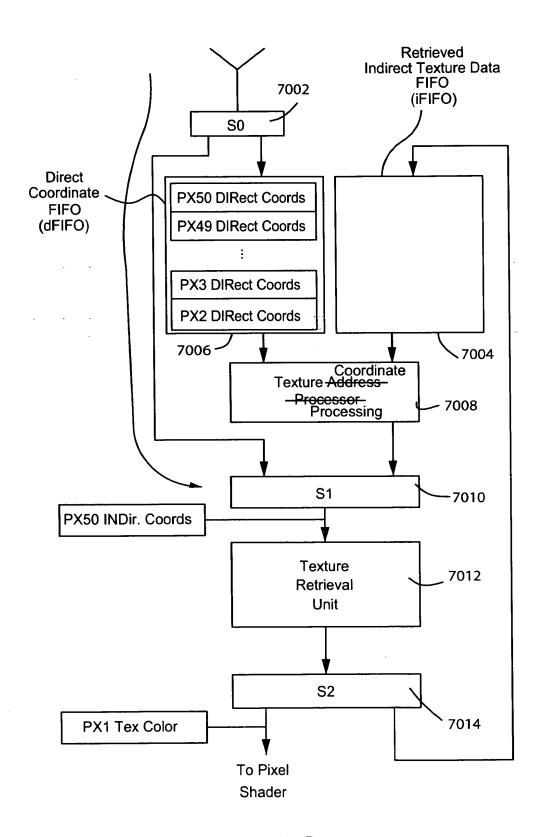


Fig. 10G

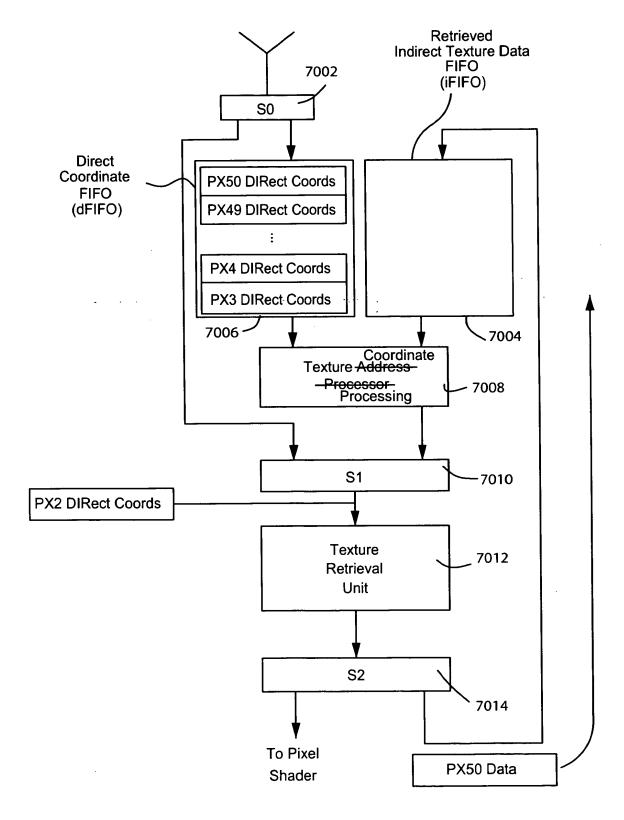


Fig. 10H

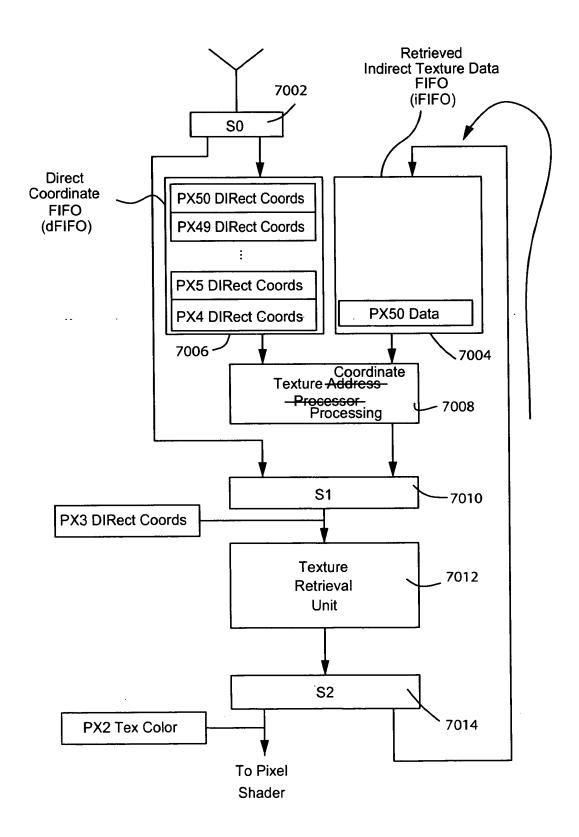


Fig. 101

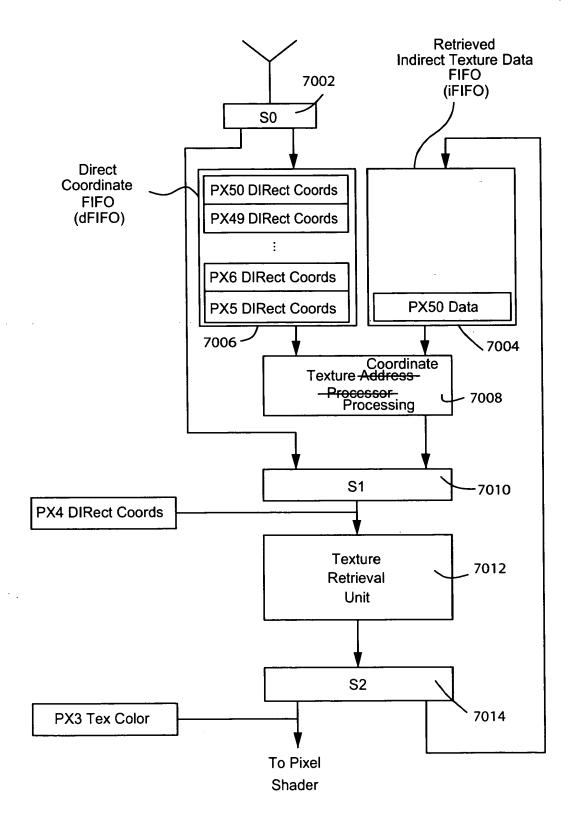


Fig. 10J

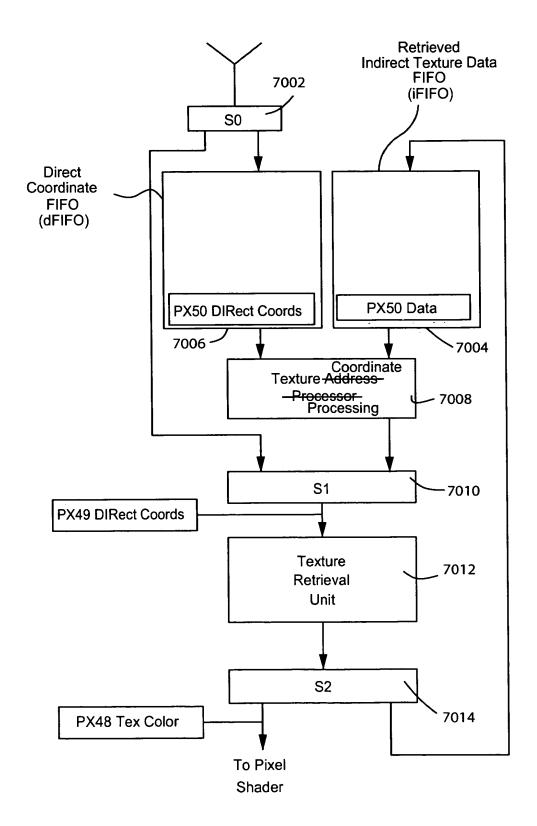


Fig. 10K

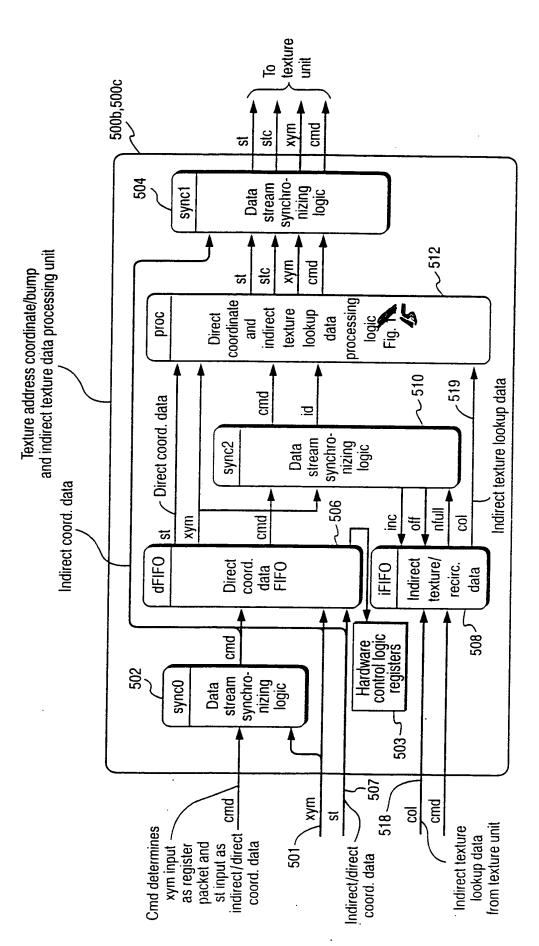
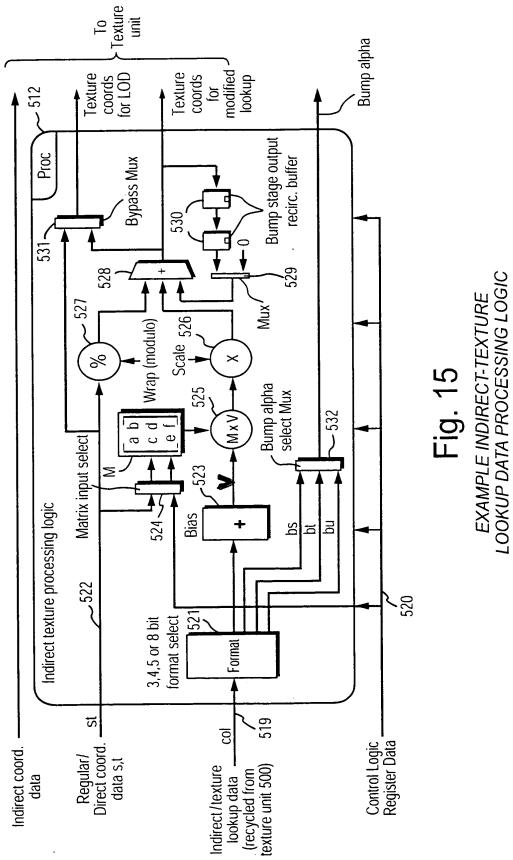


Fig. 14

EXAMPLE BUMP/TEXTURE COORDINATE PROCESSING UNIT

Appl. No. 09/722,382 Atty. Dkt.: 723-961 ANNOTATED SHEET SHOWING CHANGES



Appl. No. 09/722,382 Atty. Dkt.: 723-961 ANNOTATED SHEET SHOWING CHANGES

$MTXA_{i}$	s _i (1:0)	mb _i (10:0)			ma _i (10:0)			
$MTXB_i$	s _i (3:2)	md _i (10:0)			mc _i (10:0)			
$MTXC_i$	s _i (5:4)	mf _i (10:0)			me _i (10:0)			
CMDi		fb _i tw _i	swi	m _i	bi	as _i fmt _i	bt _i	
				•			,	
	•							
					ima	ask (7:0)		
GEN MODE		nbmp		ntev		ntex		

Fig. 17
EXAMPLE CONTROL
LOGIC REGISTERS